

## Simultaneous improvement of $J_{sc}$ , $V_{oc}$ and FF of polymer solar cells with CuI as hole transport layer

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**Abstract:** A novel buffer layer copper iodide (CuI) was introduced into PCDTBT, PC70BM polymer solar cells (PSCs), where the CuI acts simultaneously as of hole transport layer (HTL) and electron block layer (EBL). Through depositing the CuI between the polymer and Ag and Au anodes, the hole collection ability has been increased. By optimizing the thickness of CuI and top anode, simultaneous enhancement of short-circuit current density ( $J_{sc}$ ), open-circuit voltage ( $V_{oc}$ ), and fill factor (FF) has been achieved, leading to a dramatic increase of device efficiency, from 0.67% to 5.47% with 3 nm CuI and Au anode in comparison with the device without CuI. With thicker CuI, the efficiency decreases noticeably both for Au and Ag anodes due to the block effect. The result indicates that the CuI is an effective buffer layer for PCDTBT, PC70BM PSCs.

**Key words:** polymer solar cells, hole transport layer, copper iodide

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## CuI 空穴传输层提高聚合物太阳能电池 $J_{sc}$ , $V_{oc}$ 及 FF 的研究

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**摘要:** 碘化铜在器件中既是空穴传输层,又是电子阻挡层的特点,提出在 PCDTBT、PC<sub>70</sub>BM 聚合物太阳能电池中引入了碘化铜(CuI)传输层。将碘化铜淀积到顶电极银和聚合物材料之间,有效地提高了器件的空穴传输能力。实验优化了碘化铜传输层的厚度,研究了不同顶电极对聚合物太阳能电池的影响,证明了碘化铜

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能够同时提高电池的短路电流密度、开路电压和填充因子,因此得到了效率显著提高的太阳能电池。对于使用金电极的电池,碘化铜厚度为 3 nm 时,电池效率从 0.67% 提高到 5.47%,当进一步提高碘化铜厚度时,对于金、银两种电极,电池效率均由于阻挡效应而下降。实验结果表明,碘化铜是 PCDTBT、PC<sub>70</sub>BM 聚合物太阳能电池的一种有效的传输层材料。

**关键词:** 聚合物太阳能电池;空穴传输层;碘化铜

## 0 Introduction

Based on blending comprising conjugated polymers and fullerenes, polymer solar cells (PSCs) have attracted more and more attention due to its potential in lower cost renewable energy conversion compared with traditional silicon solar cells. The potential features of PSCs include easy fabrication process, large area fabricated and flexibility<sup>[1-3]</sup>. Although the power conversion efficiency (PCE) of PSCs is gradually increased, the PCE is still lower than their inorganic semiconductor counterparts because of the narrow absorption of polymers in the solar spectrum. Admittedly, the lower absorption, the lower PCE. Therefore, further improvements are required for mass production and practical application, especially simultaneous enhancement of parameters of PSC, such as short-circuit current density ( $J_{sc}$ )<sup>[4]</sup>, open-circuit voltage ( $V_{oc}$ )<sup>[5]</sup>, and fill factor (FF)<sup>[6]</sup>. For the present situation, significant investigations in PCE improvement have been conducted, including novel polymer materials design<sup>[7]</sup>, interface control engineering<sup>[8]</sup> and device engineering<sup>[9]</sup>. Among the approaches to improving the PCE, the most common and successful strategy is developing new low bandgap polymer materials to maintain a broad absorption of the solar spectrum and ensure effective harvesting of solar photons, leading to higher  $J_{sc}$ . However, since there is a trade-off between light harvesting and  $V_{oc}$ <sup>[10]</sup>, a higher PCE can be expected only if a decrease of  $V_{oc}$  can be avoided. In addition, other approaches based on device physics have also been studied and proved to be effective, yet these methods normally can only improve one or two key parameters of PSCs substantially at the same time. Beside the methods mentioned above, the interface materials engineering is important for

highly efficient and , SC devices, since adjusted interfaces can drastically improve the  $J_{sc}$ ,  $V_{oc}$  and FF simultaneously<sup>[1-13]</sup>.

In this paper, a thin copper iodide (CuI) layer is inserted into PCDTBT: PC<sub>70</sub>BM<sup>[14-16]</sup> and top anode of inverted PSCs using the vacuum deposition method. The CuI buffer layer plays an important role in the improvement of the collection efficiency of anode electrode and the extraction of hole carriers. P-type semiconductor CuI is a potential hole conductor, which has been used in dye-sensitized<sup>[17]</sup> and perovskite solar cells<sup>[18]</sup> based on its wide band gap (3.0 eV) and high conductivity. Therefore, we both optimize the CuI thickness and top anode. For both Ag and Au anodes, by optimizing the thickness of CuI, simultaneous enhancement of  $J_{sc}$ ,  $V_{oc}$ , and FF will finally be achieved. Hence, a dramatic increase of device efficiency is expected, which raised from 1.17% to 5.47% with 3 nm CuI and Au anode, compared to the device without CuI. For both Ag and Au anodes, with thicker thickness of CuI, the efficiency decrease obviously due to block effect. The result suggests that the CuI is an effective HTL buffer layer and it can be a route for improving the efficiency of PSCs.

## 1 Experimental section

The preparation of devices is described as follows: As shown in Fig. 1, the inverted PSC structure is Glass/ITO/ TiO<sub>2</sub>/PCDTBT, PC<sub>70</sub>BM/CuI (0 nm, 3 nm, 6 nm, 9 nm)/Ag and Au (80 nm). The ITO-coated glass substrates were first cleaned by acetone, ethanol and de-ionized water for 15 min, respectively. Anatase TiO<sub>2</sub> thin films were prepared by sol-gel method. PCDTBT and PC<sub>70</sub>BM (Lumtec Corp) was dissolved in 1, 2-dichlorobenzene to produce 7 mg/ml solution in 1: 4 weight ratio. The CuI (3 nm, 6 nm, 9 nm)

and 80 nm **斜体** were deposited in vacuum. The thickness of CuI is monitored by film thickness monitor. J-V characteristics were measured with Keithley 2601 source. Incident photon-to-electron conversion efficiency (IPCE) was measured with a Crowntech QTest Station 1000AD. Impedance spectroscopy was measured by an impedance analyzer (Wayne Kerr Electronics 6520B) with an ac signal of 1 V in the frequency range of 20 Hz-1 MHz.

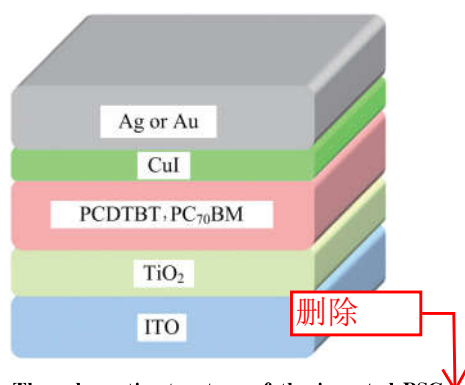


Fig.1 The schematic structure of the inverted PSCs.

## 2 Results and discussion

### 2.1 J-V characteristics and IPCE

Firstly, to optimize the thickness of the CuI HTL and anode, devices with different thicknesses of CuI (3 nm, 6 nm, 9 nm) with different anodes (Ag and Au) are fabricated. PSCs using no CuI and 3, 6, 9 nm CuI were fabricated with the following structures; Glass/ITO/ TiO<sub>2</sub>/PCDTBT, PC<sub>70</sub>BM/CuI/Ag (or Au) (Fig.1). Fig.2 shows the J-V characteristics of inverted PSCs of different devices under AM1.5 G illumination of 100 mW/cm<sup>2</sup>. The detailed results are provided in Tab.1. In both Fig.2 (a) and Fig.2 (b), the devices PCE are remarkably enhanced by the insertion of the one with 3 nm CuI for Ag and Au anode, indicating the most significant improvement in performance. Subsequently, for devices with Ag anode (Fig.2(a)), the device without CuI buffer layer shows short circuit current density ( $J_{sc}$ ) of 5.74 mA/cm<sup>2</sup>, open circuit voltage ( $V_{oc}$ ) of 0.39 V, fill factor (FF) of 28.6%, and PCE of 0.64%. When introducing the CuI into inverted PSCs, the performance is changed distinctly which is superior to devices without CuI, including  $J_{sc}$ ,  $V_{oc}$ , and

FF. The optimized thickness of CuI is 3 nm, which shows  $J_{sc}$  of 10.32 mA/cm<sup>2</sup>,  $V_{oc}$  of 0.81 V, FF of 55.7%, and PCE of 4.66%. By increasing thickness of CuI, the PCE decreased. Then, for the device with Au anode (Fig.2(b)), without the CuI buffer layer, the device shows  $J_{sc}$  of 6.75 mA/cm<sup>2</sup>,  $V_{oc}$  of 0.45 V, FF of 38.5%, and PCE of 1.17%, which are all higher than the device with Ag anode without the CuI buffer layer. The change tendency of device performance is same as that of Ag anode. The optimized thickness of CuI is also 3 nm, which shows  $J_{sc}$  of 10.85 mA/cm<sup>2</sup>,  $V_{oc}$  of 0.83 V, FF of 60.7%, and highest PCE of 5.47%. Regarding the same thickness of CuI, the device performances with Au anode are all higher than those of devices with Ag anode, indicating that the combination of CuI and Au is the best.

Tab.1 Characteristic data of devices with CuI (0 nm, 3 nm, 6 nm, 9 nm) with Ag and Au anodes

CuI	Anode	$J_{sc}$ (mA/cm <sup>2</sup> )	$V_{oc}$ (V)	FF (%)	PCE (%)	$R_s$ ( $\Omega \cdot \text{cm}^2$ )
0 nm	Ag	5.74	0.39	28.6	0.64	45.4
	Au	6.75	0.45	38.5	1.17	28.6
3 nm	Ag	10.32	0.81	55.7	4.66	12.5
	Au	10.85	0.83	60.7	5.47	11.8
6 nm	Ag	9.23	0.77	48.0	3.41	14.3
	Au	9.75	0.79	51.8	3.99	13.3
9 nm	Ag	7.64	0.65	39.4	1.96	33.9
	Au	8.24	0.69	43.3	2.46	24.8

Upon the incorporation of the 3 nm CuI HTL and Au anode, an improvement of  $J_{sc}$  from 6.75 mA/cm<sup>2</sup> to 10.85 mA/cm<sup>2</sup> was observed. Besides, the  $J_{sc}$  decreased with thicker CuI, which is too thick to block the hole transportation. As a result, the CuI can regulate the Schottky barrier and thus form an ohmic contact at the interface of the active layer and Au electrode. The photocurrent improvement is due to the collection enhancement of holes and electrons. To test the change of  $J_{sc}$ , IPCE spectra are tested. In Fig.3(a) and Fig.3(b), it is clear that the IPCE of the device without CuI is the lowest due to the poor transportation between the active layer and Ag and Au anodes.

The highest IPCE is obtained from the device with 3 nm CuI. With the same thickness of CuI, the IPCE of Au devices are higher than Ag devices, corresponding to the  $J_{sc}$  variation tendency. This considerable improvement of IPCE indicates that the charge carrier collection anode is increased by inducing a CuI HTL. When CuI is thicker than 3

nm, the IPCE decline but is also higher than the control device because of charge carrier recombination resulted from the higher  $R_s$ . The highest IPCE is obtained from the device with 3 nm CuI and Au anode, implying that the Au is superior than Ag anode for CuI HTL.

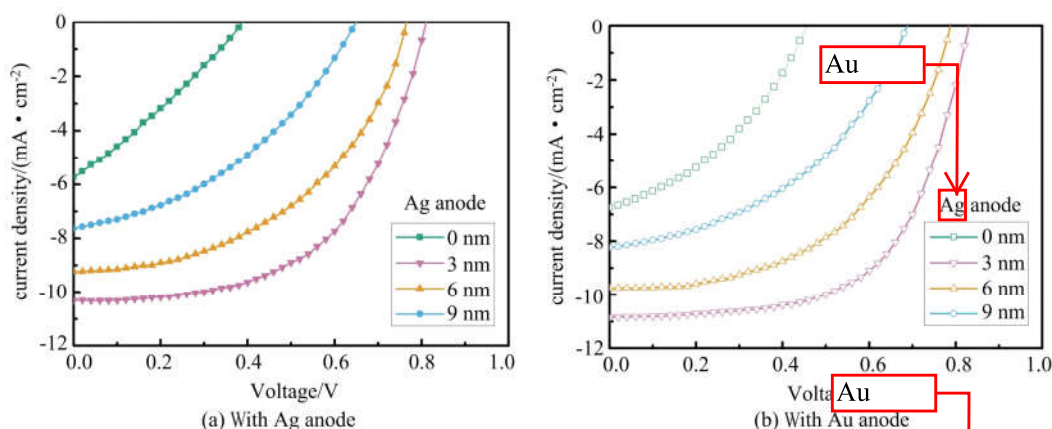


Fig.2  $J$ - $V$  characteristics of inverted PSCs with CuI (0 nm, 3 nm, 6 nm, 9 nm) under AM1.5 G illumination of 100 mW/cm<sup>2</sup>

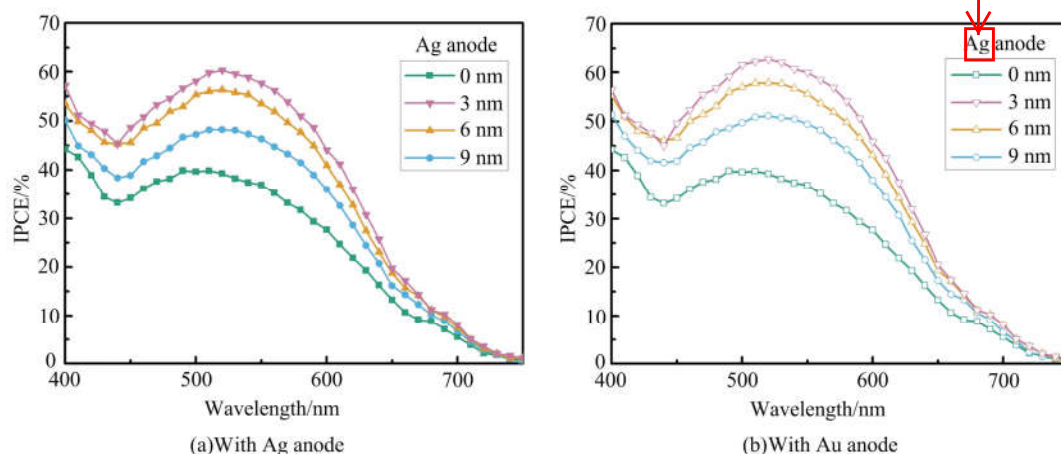


Fig.3 IPCE of inverted PSCs with CuI (0 nm, 3 nm, 6 nm, 9 nm)

## 2.2 Impedance spectra Analysis

We calculated the series resistance ( $R_s$ ) of every PSC (Tab.1). The device without CuI shows highest  $R_s$  due to contact resistance of interface of PCDTBT, PC<sub>70</sub> BM and Ag electrode. The  $R_s$  of PSCs with CuI is lower than the device without CuI both for Ag and Au anode. Besides, the lowest  $R_s$  is achieved from the device with 3 nm CuI and Au anode. Obviously, the  $R_s$  in the devices with 3 nm CuI and Au anode is the smallest which can further ensure a reduced applied bias voltage loss and improve the  $V_{oc}$ . For Ag and Au anode devices

with a thicker CuI layer, the  $R_s$  is gradually increased, leading to electrical potential improved that drops onto the active layer and interface with the electrode. Then,  $V_{oc}$  decreased. Besides the significant improvement in  $V_{oc}$ , the FF is also improved from 28.5% to 51.7% upon 3 nm CuI.

To illustrate the  $V_{oc}$  and FF improvement, the energy levels of the materials used in inverted PSCs are presented in Fig.4. The valence band of CuI buffer layer is  $-5.2\text{eV}$ <sup>[17-18]</sup>. Because the valence band of CuI is close to the energy of the highest occupied molecular orbital (HOMO) of PCDTBT, the CuI is selected as the HTL.

Meanwhile, the conduction band of CuI is higher than the lowest unoccupied molecular orbital (LUMO) of PC<sub>70</sub>BM. It suggests the CuI can also play the role of an electron block layer (EBL). Thus, the hole can be efficiently transported to the Ag anode and electron can be simultaneously blocked. For different anodes, the work function for Au is lower than Ag. The  $V_{oc}$  enhancement is attributed to the change of built-in potential.

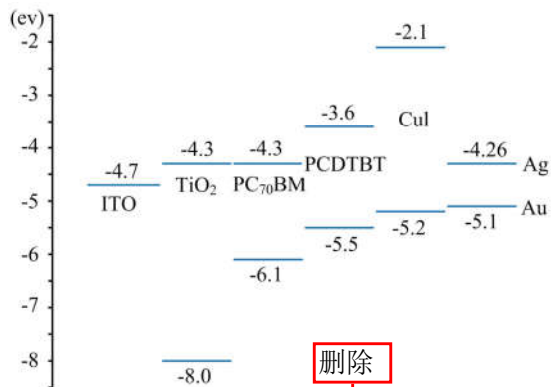


Fig.4 Energy levels of the materials used in inverted PSCs

The impedance spectra of PSCs with CuI (0 nm, 3 nm, 6 nm, 9 nm) and Au anode were measured in the dark Nyquist diagram with frequency ranging from 20 Hz to 1 MHz (Fig. 5) by an impedance analyzer (Wayne Kerr Electronics 6520 B). Impedance spectrum is a powerful tool to investigate the interface and bulk electronic properties of PSC<sup>[19-20]</sup>. Besides, the equivalent model of the device is also shown in Fig. 5. The shunt pair with  $R_1$  and  $C_1$  corresponds to the active layer, which is usually called “diffusion capacitance” or “chemical capacitance”. The shunt pair with  $R_2$  and  $C_2$  corresponds to the electrical contacts of the interfaces between TiO<sub>2</sub>/PCDTBT, PC<sub>70</sub>BM and PCDTBT:PC<sub>70</sub>BM/CuI. The  $R_3$  corresponds to the electrodes including the resistance of ITO, TiO<sub>2</sub>, CuI, and Au. The shape of impedance spectra are both semicircles that are beneficial to investigate the interface resistance in PSCs. For the control device without CuI, the semicircle is bigger than the device with CuI. The largest diameter (resistance) of the device without CuI is about  $0.28 \Omega \text{ m}^2$ . The smallest semicircle is achieved with 3 nm CuI, of which the diameter (resistance) is about  $0.02 \Omega \text{ m}^2$ . Though increasing

the CuI thickness, the diameter (resistance) is larger than the 3 nm CuI device, yet it is still lower than that of the control device. Due to the high sensitivity of the resistance to the CuI thickness, it can be concluded that the semicircles observed in the impedance spectra are caused by the Ag/PCDTBT, PC<sub>70</sub>BM interface. The tendency of impedance spectra has exact accordance with the  $JV$  data for devices with different thicknesses of CuI.

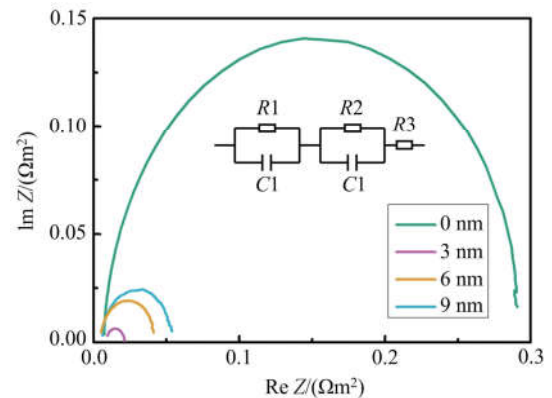


Fig.5 Impedance spectra of the devices with CuI (0 nm, 3 nm, 6 nm, 9 nm) in the dark at 0 V. Inset: equivalent RC circuit of the PSCs in the dark with Au anode

### 3 Conclusion

In conclusion, we have demonstrated that it is possible to incorporate a CuI layer to improve the  $J_{sc}$ ,  $V_{oc}$  and FF of PCDTBT, PC<sub>70</sub>BM PSC at the same time. Moreover, the CuI are located adjacent to the hole collecting anode and polymer layer, which are typically considered as efficient HTL and EBL. In this paper, we optimized the thickness of CuI and anode, which is critical for device performance by influencing the  $R_s$  and  $V_{oc}$ . Efficient inverted PSCs were achieved with 3 nm CuI/Au anode. By incorporating CuI, the ability of hole collection was increased at the same time. The  $V_{oc}$  of 0.83 V,  $J_{sc}$  of  $10.85 \text{ mA/cm}^2$  and FF of 60.7% for the PSC with 3 nm CuI as HTL were obtained with PCE as high as 5.47%. The results demonstrate that the CuI is an effective buffer layer with Au anode in PCDTBT, PC<sub>70</sub>BM PSCs and the approach reported here provides a simple and effective method for the optimization of PSC.



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